EC 521: LOW POWER VLSI DESIGN (3-0-2:4)

Physics of Power Dissipation in CMOS FET Devices
Physics of power dissipation in MOSFET devices, power dissipation in cmos, low power vlsi design: Limits

Power Estimation

Synthesis for Low Power
Behavioral Level Transforms, Logic Level Optimization for Low power, Circuit Level Optimization.

Design and Test of Low Voltage CMOS Circuits
Circuit Design style, Leakage current in deep submicrometer transistors, Deep submicrometer device design issues, Key to minimizing SCE, Low voltage circuit design techniques, Designing deep submicrometer ics with elevated intrinsic leakage, multiple supply voltages.

Low Power Static RAM Architectures
Organization of a static RAM, MOS Static RAM Memory cell, Banked organization of SRAMs, Reducing voltage swings on bit lines, Reducing power in write driver circuits, Reducing power in sense amplifier circuits, method for achieving low core voltages from a single supply.

Low Energy Computing using Energy Recovery Techniques
Energy dissipation in transistor channel using an RC model, Energy recovery circuit design, Designs with partially reversible logic, Supply clock generation.

Suggested list of Experiments:
1. Low power Adders
2. Power delay measurement of Adders
3. Low power Multipliers
4. Power delay measurement of Multipliers

Text Books and References